Abstract of the Disclosure

The present invention relates to an ultra small size vertical MOSFET device having a vertical channel and a source/drain structure and a method for the manufacture thereof by using a silicon on insulator (SOI) substrate. To begin with, a first silicon conductive layer is formed by doping an impurity of a high concentration into a first single crystal silicon layer. Thereafter, a second single crystal silicon layer with the impurity of a low concentration and a second silicon conductive layer with the impurity of the high concentration are formed on the first silicon conductive layer. The second single crystal silicon layer and the second silicon conductive layer are vertically patterned into a predetermined configuration. Subsequently, a gate insulating layer is formed on entire surface. Then, an annealing process is carried out to diffuse the impurities in the first silicon conductive layer and the second silicon conductive layer into the second single crystal layer, thereby forming a source contact, a drain contact and a vertical channel. Finally, a gate electrode is formed on side walls of the vertical channel.